ABSTRACT

A semiconductor integrated circuit device is provided with a diagnosis circuit, which does not increase the delay of a logic element in normal operation. In a latch provided at the output of a memory or at the input of a logic stage, a signal selector is provided in the feedback loop of the latch. The selector is switched in correspondence with the operation mode, such that it transfers the feedback signal in normal operation, while it transfers the test signal in a test mode, in order to prevent the delay from increasing in the signal selector on the main path in normal operation.